深圳市海凌科电子有限公司

SHENZHEN HI-LINK ELECTRONIC CO.,LTD.

HLK-7621A User manual/使用手册

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目　录

CATALOG

1. Introdution

1.1. General

The HLK-7621A module use the MT7621A chipset.The MT7621A integrates aual-core MIPS-1004Kc (880MHz), HNAT/HQoS/Samba/VPN accelerators, 5-port GbE switch, RGMII, USB3.0, USB2.0, 3xPCIe, SD-XC. The powerful CPU with rich portfolio is suitable for 802.11ac, LTE cat4/5, edge, hotspot, VPN,AC (Access Control). It can also connect to touch-panel, ZigBee/Z-Wave for Internet Service Router and Home Security Gateway.

For the next generation router, MT7621A provides several dedicated hardware engines to accelerate the NAT, QoS, Samba and VPN traffic.These accelerators relief the CPU for other upper layer applications.

1.2. Features

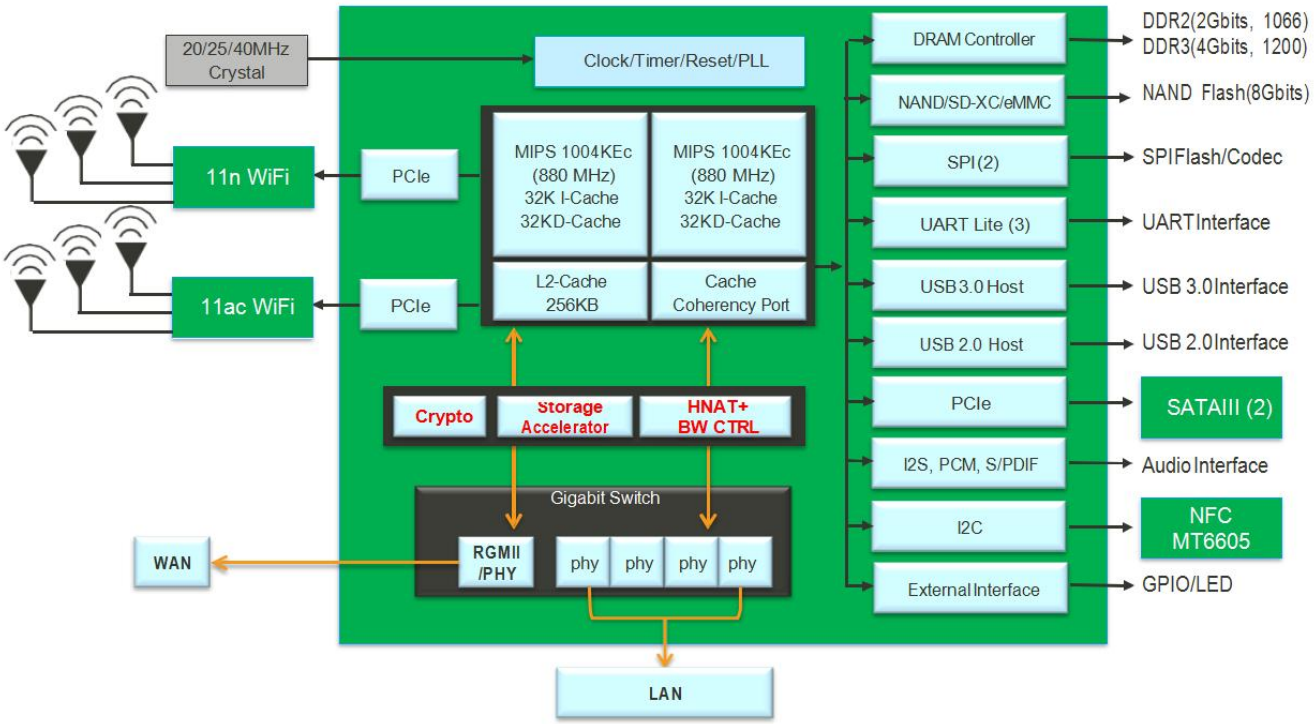
- Embedded MIPS1004Kc (880 MHz, Dual-Core)
  - - 32 KB I-Cache and 32 KB D-Cache per core
  - - 256 KB L2 Cache (shared by Dual-Core
  - - SMP capable
  - - Single processor operation configurable
- Gigabit Switch
  - - 5 ports with full-line rate
  - - 5-port 10/100/1000Mbps MDI transceivers
- One RGMII/MII interface
- 16-bit DDR2/3 up to 256/512 Mbytes
- SPI(2 chip select), NAND Flash(SLC), SDXC,eMMC(4 bits)
- USB3 x 1+ USB2 x 1 or USB2 x 2 (all host)
- PCIe host x 3
- I2C, UART Lite x 3, JTAG, MDC, MDIO, GPIO
- VoIP support (I2S, PCM)
- Audio interface (SPDIF-Tx, I2S, PCM)
- Deliver the superb Samba performance via USB2.0/USB 3.0/SD-XC
- HW storage accelerator
- HW NAT
  - - 2Gbps wired speed
  - - L2 bridge
  - - IPv4 routing, NAT, NAPT
  - - IPv6 routing, DS-Lite, 6RD, 6to4
- HW QoS
  - - 16 hardware queues to guarantee the min/max bandwidth of each flow.
  - - Seamlessly co-work with HW NAT engine.
  - - 2Gbps wired speed.
- HW Crypto
- Deliver 400~500 Mbps IPSec throughput

- Green
  - -Intelligent Clock Scaling (exclusive)
  - -DDR2/3: ODT off, Self-refresh mode
- Firmware: Linux 2.6 SDK, OpenWRT
- RGMII iNIC Driver: Linux 2.4/2.6

2. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-40	125	℃
Ambient Operating Temperature	-40	85	℃
Junction Temperature	-40	85	℃

3. Functional Block Diagram



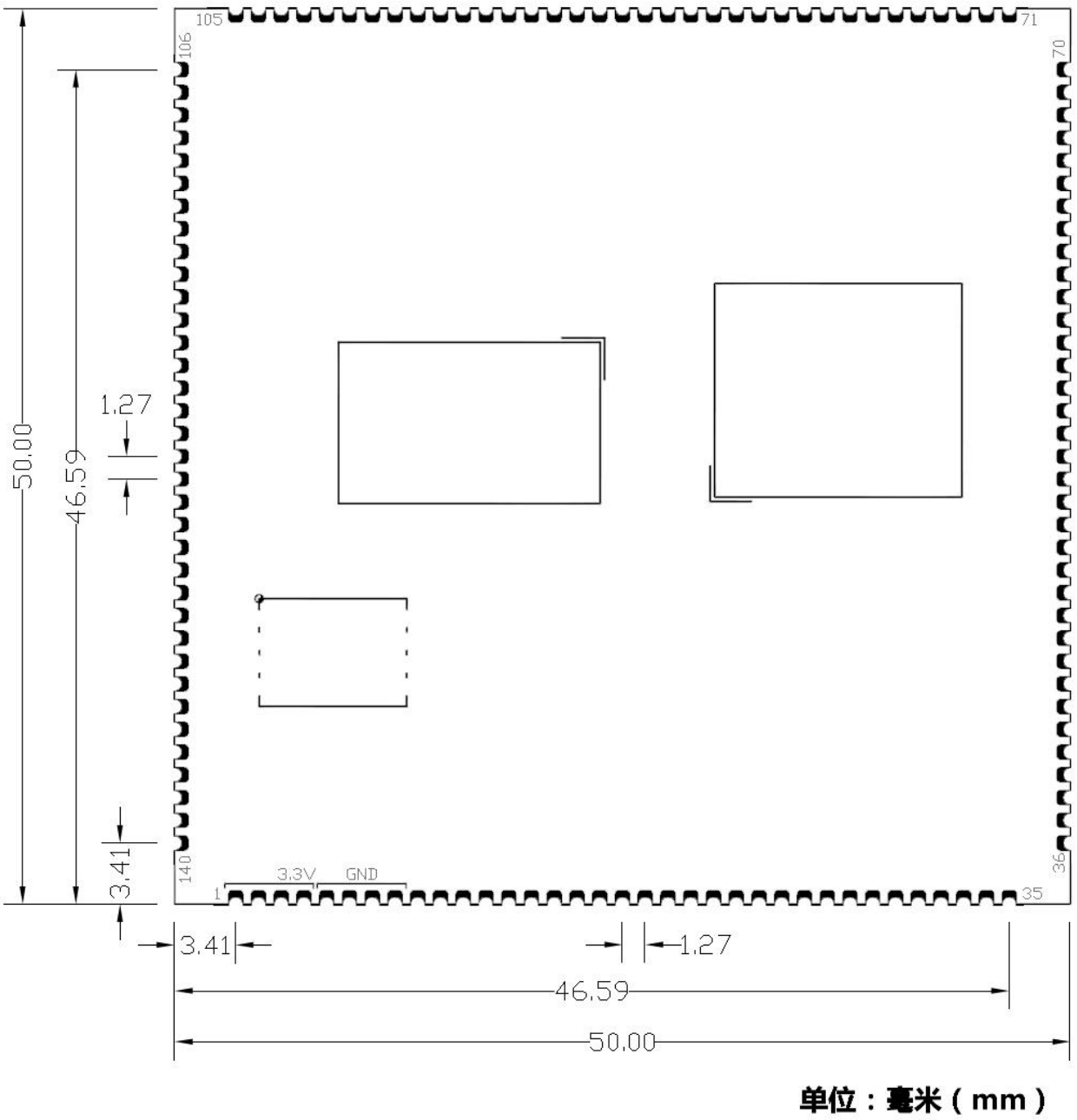
4. Electrical Specifications

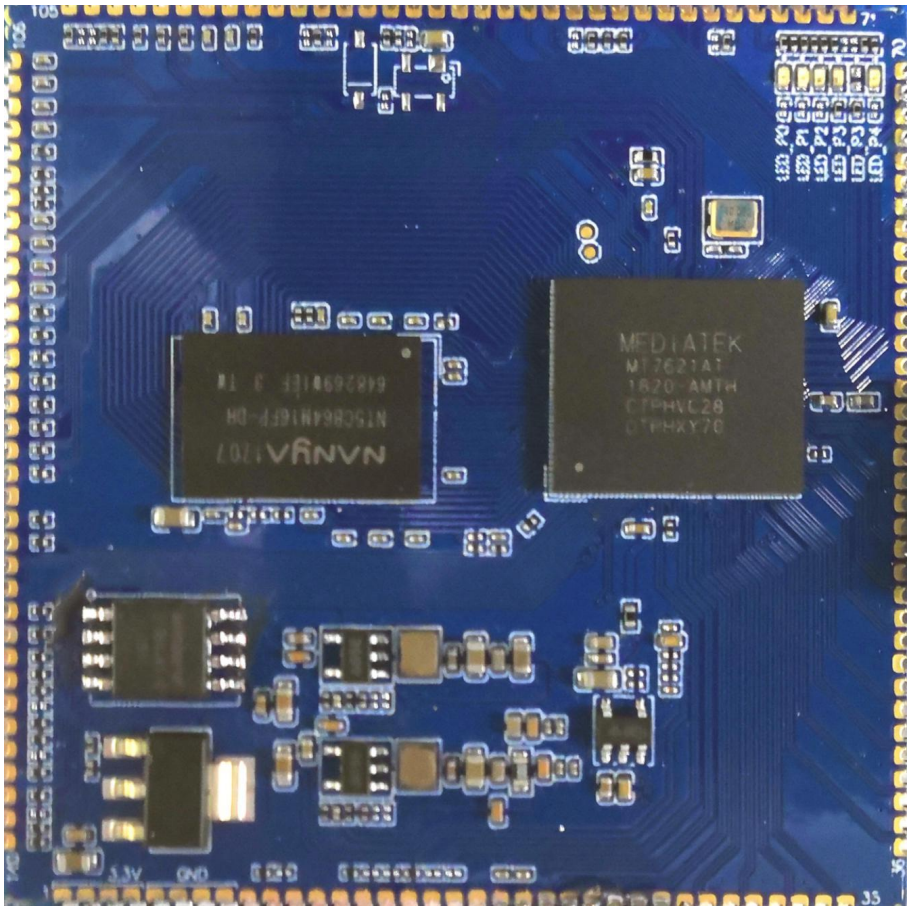
DC Characteristics

Module	Voltage	Design requirements
HLK-7621	3.3V	500mA

5. Mechanical

Dimensions (mm)	Length	Width	Height
	50 (Tolerance: ±0.2mm)	**50** (Tolerance: ±0.2mm)	**3** (Tolerance: ±0.2mm)





HLK-7621

6. Pins Description

Pin	Function	Descriptionion
1	3.3VD	POWER
2	3.3VD	POWER
3	3.3VD	POWER
4	3.3VD	POWER
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	CTS3_N	UART Clear To Send
10	TXD2	UART TX Data
11	RXD2	UART RX Data
12	TXD3	UART TX Data

13	RXD3	UART RX Data
14	RTS2_N	UART Request To Send
15	CTS2_N	UART Clear To Send
16	RTS3_N	UART Request To Send
17	USB_DP_1P	USB Port1 data pin Data+ (USB2.0)
18	USB_DM_1P	USB Port1 data pin Data- (USB2.0)
19	GND	Ground
20	SSUSB_TXP	USB Port0 SS data pin TX+ (USB3.0)
21	SSUSB_TXN	USB Port0 SS data pin TX- (USB3.0)
22	SSUSB_RXP	USB Port0 SS data pin RX+ (USB3.0)
23	SSUSB_RXN	USB Port0 SS data pin RX+-(USB3.0)
24	GND	Ground
25	USB_DP_P0	SB Port0 HS/FS/LS data pin Data+ (USB3.0)
26	USB_DM_P0	USB Port0 HS/FS/LS data pin Data- (USB3.0)
27	GND	Ground
28	ESW_TXVP_A_P0	Port #0 MDI Transceivers
29	ESW_TXVN_A_P0	Port #0 MDI Transceivers
30	ESW_TXVP_B_P0	Port #0 MDI Transceivers
31	ESW_TXVN_B_P0	Port #0 MDI Transceivers
32	ESW_TXVP_C_P0	Port #0 MDI Transceivers
33	ESW_TXVN_C_P0	Port #0 MDI Transceivers
34	ESW_TXVP_D_P0	Port #0 MDI Transceivers
35	ESW_TXVN_D_P0	Port #0 MDI Transceivers
36	ESW_TXVP_A_P1	Port #1 MDI Transceivers
37	ESW_TXVN_A_P1	Port #1 MDI Transceivers
38	ESW_TXVP_B_P1	Port #1 MDI Transceivers
39	ESW_TXVN_B_P1	Port #1 MDI Transceivers
40	ESW_TXVP_C_P1	Port #1 MDI Transceivers
41	ESW_TXVN_C_P1	Port #1 MDI Transceivers
42	ESW_TXVP_D_P1	Port #1 MDI Transceivers
43	ESW_TXVN_D_P1	Port #1 MDI Transceivers
44	GND	Ground

45	ESW_TXVP_A_P2	Port #2 MDI Transceivers
46	ESW_TXVN_A_P2	Port #2 MDI Transceivers
47	ESW_TXVP_B_P2	Port #2 MDI Transceivers
48	ESW_TXVN_B_P2	Port #2 MDI Transceivers
49	ESW_TXVP_C_P2	Port #2 MDI Transceivers
50	ESW_TXVN_C_P2	Port #2 MDI Transceivers
51	ESW_TXVP_D_P2	Port #2 MDI Transceivers
52	ESW_TXVN_D_P2	Port #2 MDI Transceivers
53	GND	Ground
54	ESW_TXVP_A_P3	Port #3 MDI Transceivers
55	ESW_TXVN_A_P3	Port #3 MDI Transceivers
56	ESW_TXVP_B_P3	Port #3 MDI Transceivers
57	ESW_TXVN_B_P3	Port #3 MDI Transceivers
58	ESW_TXVP_C_P3	Port #3 MDI Transceivers
59	ESW_TXVN_C_P3	Port #3 MDI Transceivers
60	ESW_TXVP_D_P3	Port #3 MDI Transceivers
61	ESW_TXVN_D_P3	Port #3 MDI Transceivers
62	GND	Ground
63	ESW_TXVP_A_P4	Port #4 MDI Transceivers
64	ESW_TXVN_A_P4	Port #4 MDI Transceivers
65	ESW_TXVP_B_P4	Port #4 MDI Transceivers
66	ESW_TXVN_B_P4	Port #4 MDI Transceivers
67	ESW_TXVP_C_P4	Port #4 MDI Transceivers
68	ESW_TXVN_C_P4	Port #4 MDI Transceivers
69	ESW_TXVP_D_P4	Port #4 MDI Transceivers
70	ESW_TXVN_D_P4	Port #4 MDI Transceivers
71	ESW_P4_LED_0	Port #4 PHY LED indicators
72	ESW_P3_LED_0	Port #3 PHY LED indicators
73	ESW_P2_LED_0	Port #2 PHY LED indicators
74	ESW_P1_LED_0	Port #1PHY LED indicators
75	ESW_P0_LED_0	Port #0 PHY LED indicators
76	ESW_DTEST	Digital test

77	GE2_TXD3	RGMII2 Tx Data bit #0
78	GE2_TXD2	RGMII2 Tx Data bit #2
79	GE2_TXD1	RGMII2 Tx Data bit #1
80	GE2_TXD0	RGMII2 Tx Data bit #0
81	ESW_DBG_B	
82	MDIO	PHY Management Data. Note: While RGMII/MII connects to external PHY, this pin is MDIO. Else, it should be NC.
83	MDC	PHY Management Clock. Note: While RGMII/MII connects to external PHY, this pin is MDC. Else, it should be NC.
84	GE2_TXEN	RGMII2 Tx Data Valid
85	GE2_TXCLK	RGMII2 Tx Clock
86	GE2_RXD3	RGMII2 Rx Data bit #3
87	GE2_RXD2	RGMII2 Rx Data bit #2
88	GE2_RXD1	RGMII2 Rx Data bit #1
89	GE2_RXD0	RGMII2 Rx Data bit #0
90	GE2_RXDV	RGMII2 Rx Data Valid
91	GE2_RXCLK	RGMII2 Rx Clock
92	GND	Ground
93	RXD1	UART TX Data
94	TXD1	UART RX Data
95	PORST_N	Power on reset
96	I2C_SCLK	I2C Clock
97	I2C_SD	I2C Data
98	PCIE_TXN2	PCIE2_TX-
99	PCIE_TXP2	PCIE2_TX+
100	PCIE_RXN2	PCIE2_RX-
101	PCIE_RXP2	PCIE2_RX+
102	PCIE_CKN2	PCIE2_CLK-
103	PCIE_CKP2	PCIE2_CLK+
104	GPIO0	
105	PERST_N	PCIE
106	PCIE_TXP1	PCIE1_TX+

107	PCIE_TXN1	PCIE1_TX-
108	PCIE_RXP1	PCIE1_RX+
109	PCIE_RXN1	PCIE1_RX-
110	PCIE_CKN1	PCIE1_CLK-
111	PCIE_CKP1	PCIE1_CLK+
112	WDT_RST_N	NC
113	PCIE_RXP0	PCIE0_RX+
114	PCIE_RXN0	PCIE0_RX-
115	PCIE_TXN0	PCIE0_TX-
116	PCIE_TXP0	PCIE0_TX+
117	PCIE_CKP0	PCIE0_CLK+
118	PCIE_CKN0	PCIE0_CLK-
119	GND	Ground
120	JTMS	JTAG Mode Select
121	JTDO	JTAG Data Output
122	JTDI	JTAG Data Input
123	JTRST_N	JTAG Target Reset
124	JTCLK	JTAG Clock
125	GND	Ground
126	ND_D7	NAND Flash Data7
127	ND_D6	NAND Flash Data6
128	ND_D5	NAND Flash Data5
129	ND_D4	NAND Flash Data4
130	ND_D3	NAND Flash Data3
131	ND_D2	NAND Flash Data2
132	ND_D1	NAND Flash Data1
133	ND_D0	NAND Flash Data0
134	ND_RB_N	NAND Flash Ready/Busy
135	ND_RE_N	NAND Flash Read Enable
136	ND_CS_N	NAND Flash Chip Select
137	ND_CLE	NAND Flash Command Latch Enable
138	ND_ALE	NAND Flash ALE Latch Enable
139	ND_WE_N	NAND Flash Write Enable

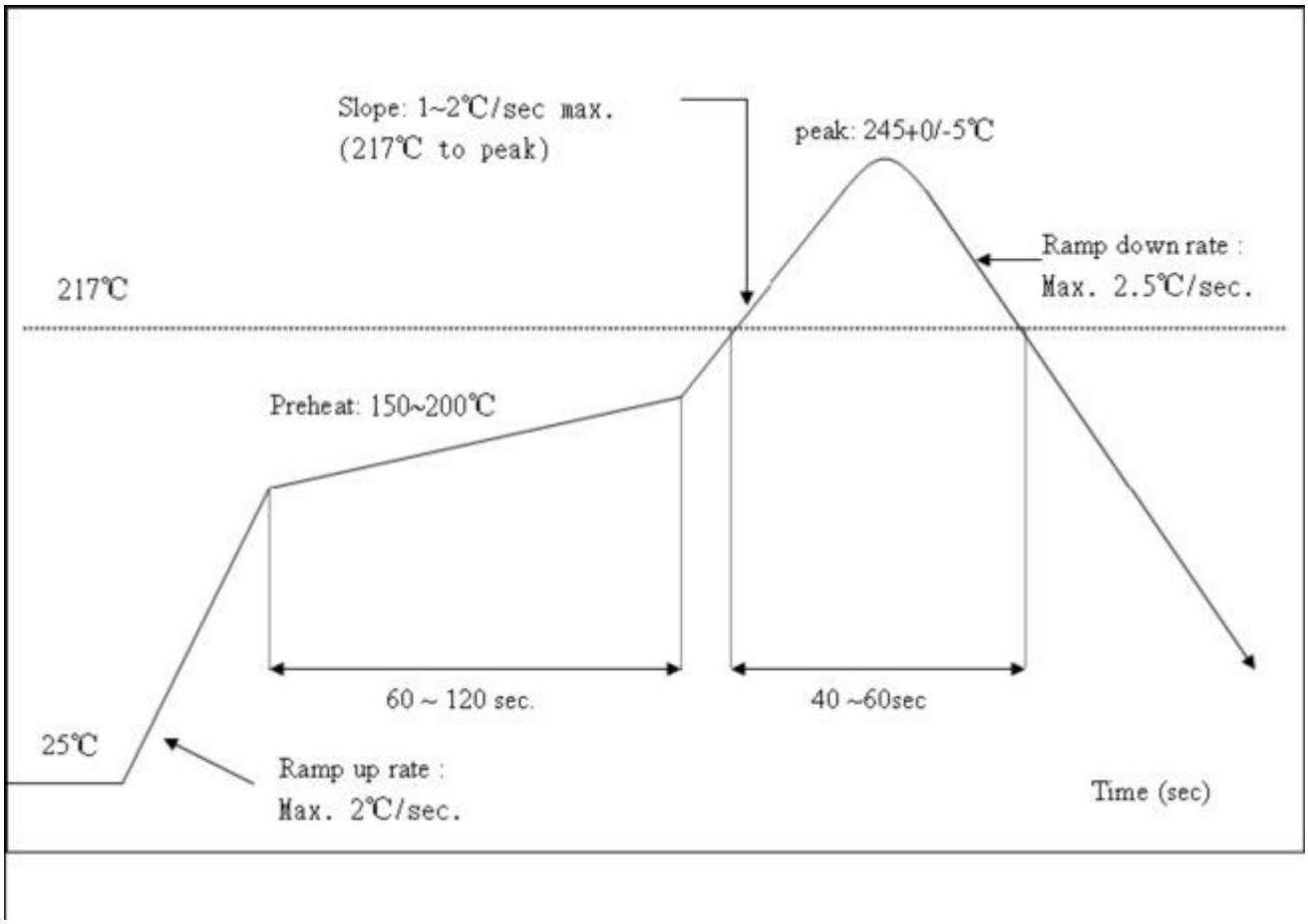
140	ND_WP	NAND Flash Write Protect

7. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times :≤2 times



8. ENVIRONMENTAL

8.1. Operating

Operating Temperature: 0°C to +60 °C

Relative Humidity: 5-90% (non-condensing)

8.2. Storage

Temperature: -10°C to +80°C (non-operating)

Relevant Humidity: 5-95% (non-condensing)

8.3. MTBF caculation

Over 150,000hours

9. Precautions before surface mounting:

⑴When customers Open stencil,theymust be sure the holeenoughbigger to the module plate, please press 1to0.7 mm is widened to open outward andthe thickness of 0.12 mm .

⑵whenweneed get the wifi module ,we can'tDirect hand andmustwear the gloves and static ring.

⑶According to the size of the customer 'sthe mainboard ,the furnace temperaturecan stick on a tablet standard temperature of250 or so up and down no more than 5 degrees and sometimes it even can achieve 260 or so up and down no more than 5 degrees.

⑷Storage and use module control should pay attention to the following matters:

a.The calculated shelf life in a sealed bag is 12 months,stored between 0 °C and 40 °C at less than90% relative humidity (RH).

b.After the bag is opened, devices that are subjected to solder reflow orother high temperature processes must be handled in the following manner:

1，Mounted within 168 hours of factory conditions, i.e. < 30°C at 60% RH.

2，Storage humidity needs to maintained at < 10% RH.

3，Baking is necessary if the customer exposes the component to air for over 168 hrs, baking conditions: 125°C for 8 hours.